UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,727	01/29/2002	Luan Tran	MCT.0004C1US	7665

7590 06/18/2003

Timothy N. Trop
TROP, PRUNER, HU & MILES
Suite 100
8554 Katy Freeway
Houston, TX 77024

EXAMINER	
FENTY, JESSE A	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/059,727	TRAN ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 of U.S. Patent No. 6,410,948 B1 in view of Chu et al. (U.S. Patent No. 5,107,459).

In re claims 1-25, Tran et al. (claim 16) discloses a semiconductor device wherein the bit lines are coupled to the sense amplifiers in a folded bit line arrangement, but does not expressly disclose each bit line including a first level portion and a second level portion.

Chu discloses bit lines (BL1 and BL2) vertically twisted from one level portion to a second level portion in a folded bit-line array. It would have been obvious to one skilled in the art at the time of the invention to configure the device of Tran in the manner disclosed by Chu for the purpose, for example of achieving a higher density memory cell architecture (Chu; Abstract).

Though Tran (claim 16) discloses the bit lines weaving with respect to the active area lines, such weaving is not necessary and it would have been obvious for one skilled in the art at the time of the invention to not weave the two lines together because a memory cell only requires one intersection between an active area line and a bit line.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 and 10-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. Patent No. 5,747,844) in view of Chu et al. (U.S. Patent No. 5,107,459).

In re claims 1, 10-12, and 17-19, Aoki (Fig. 6) discloses a semiconductor device, comprising:

Memory cells each having an area of about $6F^2$;

Sense amplifiers;

Active area lines (2), transistors being formed in the active area lines and electrically coupling corresponding memory cells to corresponding first level bit lines; and

Bit lines (BL1, BL2, ..) coupled to the sense amplifiers in a folded bit line configuration, each bit line including a first level portion and a second level portion, but does not expressly disclose each bit line being on a separate level.

Chu discloses bit lines (BL1 and BL2) vertically separated from one level to another in a folded bit-line array. It would have been obvious to one skilled in the art at the time of the invention to configure the device of Tran in the manner disclosed by Chu for the purpose, for example of achieving a higher density memory cell architecture (Chu; Abstract).

In re claims 2, 13 and 20, Aoki in view of Chu discloses the devices of claims 1, 11 and 19 respectively, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

In re claim 3, Aoki in view of Chu discloses the device of claim 2, wherein a column pitch of each memory cell is 2F.

In re claims 4, 14 and 21, Aoki in view of Chu discloses the devices of claims 1, 12 and 20 respectively, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

In re claims 5, 15 and 22, Aoki in view of Chu discloses the devices of claims 4, 14 and 21, wherein the second level portion of each bit line is formed over each capacitor.

In re claims 6 and 16, Aoki in view of Chu discloses the devices of claims 1 and 11 respectively, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions.

In re claim 7, Aoki in view of Chu discloses the device of claim 6, wherein the active area lines are generally straight and the bit lines extend in a wavy pattern.

In re claim 8, Aoki in view of Chu discloses the device of claim 6, wherein the bit lines are generally straight and the active area lines extend in a wavy pattern.

In re claim 10, Aoki in view of Chu discloses the device of claim 6, wherein the bit lines extend along generally the same direction as the active area lines so that the bit lines and active area lines intersect at predetermined locations.

In re claims 23, 24 and 25, Aoki in view of Chu discloses the devices of claims 1, 11 and 18 respectively, wherein in the folded bit line arrangement a pair of bit lines is coupled to a same side of each corresponding sense amplifier.

Response to Arguments

5. Applicant's arguments filed 03/19/03 have been fully considered but they are not persuasive.

Applicant argues that Aoki teaches away from the present invention. That a reference appears to teach away from the claims in an application, does not preclude a reference from being used as prior art. Aoki is helpful to give a perspective of the dimensional limitations of open and folded bit line configuration memory devices at the time at the filing date of 07/16/93. Those skilled in the art will recognize that semiconductor devices continue to get smaller and smaller. What was once inconceivable in terms of device size is now commonplace. Keeth et al. (U.S. 2003/0071295) originally filed 09/20/95 discloses folded bit line memory devices approaching the $6F^2$ dimenstion (pp. 7, section [0099-0100]).

The instant application now reaches the desired dimension. Examiner argues that the prior art obviates the claims. Folded bit line configurations coupled to sense amplifiers are well known device structures in the art. That the instant application now claims a smaller dimension does not constitute patentable subject matter since it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Examiner re-asserts the motivation cited in the original office action; that arranging the device of Tran et al. (U.S. Patent No. 6,410,948 B1) in the folded-bit line configuration of Chu, stacking levels on top of one another, would achieve the purpose of a higher density memory cell architecture.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty
Examiner
Art Unit 2815

JAF
June 16, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800